THIN FILM TRANSISTOR MATRIX AND ITS MANUFACTURE

Publication number: JP4334061

Publication date: 1992-11-20

Inventor:

TANAKA TSUTOMU; YANAI KENICHI; OGATA

HIROSHI; TANAKA TOSHIICHI

Applicant:

FUJITSU LTD

Classification:

- international:

G02F1/1343; G02F1/136; G02F1/1368; H01L21/336; H01L27/12; H01L29/78; H01L29/786; G02F1/13; H01L21/02; H01L27/12; H01L29/66; (IPC1-7):

G02F1/1343; G02F1/136; H01L27/12; H01L29/784

- European:

Application number: JP19910102996 19910509 **Priority number(s):** JP19910102996 19910509

Report a data error here

Abstract of JP4334061

PURPOSE:To obtain a thin film transistor matrix having a structure wherein the short circuit between data bus lines and gate bus lines and the disconnection of the gate bus lines are not generated. CONSTITUTION:The following are provided; a transparent insulative substrate 1, a transparent insulative layer 3 covering the substrate 1, and a plurality of parallel data bus lines 6 buried in the insulative layer 3 in the manner in which the height of the surface becomes nearly equal to the height of the surface of the insulative layer 3. A device is constituted of the following; a drain electrode 7 and a source electrode 8 laminated in order on the transparent insulative layer 3, an operating semiconductor layer 10, gate insulating layers 11, 12, a gate electrode 13, and a thin film transistor matrix having a plurality of parallel gate bus lines 14 perpendicularly intersecting a plurality of the parallel data bus lines 6.

Data supplied from the esp@cenet database - Worldwide